Appln. No.: 09/775,676

Amendment Dated June 24, 2004

Reply to Office Action of October 23, 2003

## **Remarks/Arguments:**

Claims 1-12 are pending. Claims 1-12 stand rejected.

## Rejections Under 35 U.S.C. § 103

The Office Action at page 2 sets forth, "claims 1, 5-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,667,149 to Cohen et al. in view of U.S. Patent No. 4,423,373 to Le Croy." Applicants respectfully submit that this rejection is overcome by the amendments to the claims for the reasons set forth below.

Applicants' invention, as recited in claim 1, includes figures which are neither disclosed nor suggested by either Cohen et al. or Le Croy, namely:

A single probe apparatus for testing a circuit chip. . .

. . .said single probe apparatus comprising a single probe group having two or more probes, said two or more probes <u>having a common</u> contacting center within a probe target area, and each of said two or more probes independently conductively contacting within a guided boundary a single test terminal of said circuit chip. . .

. . .allowing a test path resistance of said single test terminal to be measured based solely between said probes of said single probe group without affecting said circuit chip. (emphasis added)

These features are described in Applicants' specification, for example, at page 10, line 8 through page 11, line 15, page 12, line 15 through page 13, line 22, and page 15, lines 11-29.

Cohen et al. is relied upon as "[disclosing] a probe apparatus and method for testing a circuit chip/semiconductor...comprising a probe group having two or more probes...and allowable a test path resistance to be measured without affecting circuit chip/semiconductor... and probes for conductively contacting a single terminal of a chip/semiconductor..." Office Action at page 2. The Office Action readily admits, however, "Cohen et al. does not disclose two or more probes within a guiding boundary for independently conductively contacting a single terminal of a chip." To make up for this deficiency, Le Croy is relied upon as "[disclosing] that it is well known for probe apparatuses to include a guided boundary for a probe group having two or more probes...for independently conductively contacting a single terminal of a chip/semiconductor device." Neither Cohen et al. or Le Croy disclose, however, a single probe

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apparatus having two or more probes with each of the two or more probes independently conductively contacting within a guided boundary a single test terminal of a circuit chip for allowing a test path resistance of the single test terminal to be measured based solely between the probes of the single probe group. Rather, Cohen requires two probes (15 and 25) each containing two tips (14/24 and 16/24, respectively) in order for measurements to be affected. Column 4, lines 39-56 and Fig. 1. Additionally, Cohen et al. requires four single probes spaced apart from one another over an expanse of a metal under test in order to determine resistivity of the metal with current being applied at the outer probes and a voltage measured across the inner probes. Column 3, lines 14-25.

In contrast, Applicants' invention recites a <u>single</u> probe apparatus for testing a circuit chip in which the <u>single</u> probe apparatus comprises a single probe group having two or more probes having a common contacting center within a probe target area with each of the two or more probes independently conductively contacting within the guided boundary a single test terminal of a circuit chip allowing a test path resistance of the single test terminal to be measured based solely between the probes of the single probe group with affecting the circuit chip.

It is <u>because</u> Applicants have provided a single probe apparatus having a single probe group with two or more probes where each of the two or more probes have a common contacting center within a probe target area with each of the two or more probes independently conductively contacting within the guided boundary a single test terminal of the test chip, allowing for test path resistance of the single test terminal to be measured based solely between the probes of the single probe group, that Applicants are able to recognize resistance discrepancies in probe/terminal interfaces and for correspondingly adjusting a voltage level of consecutive operational signal applied onto or derived from the chip terminal during actual chip testing. Neither Cohen et al. nor Le Croy are able to achieve this advantage because Le Croy requires multiple test probes to be used and Cohen et al. admittedly lacks the grouping of multiple probes within a single probe group.

For the reasons set forth above, neither Cohen et al. nor Le Croy alone or in combination disclose every feature of Applicants' claim 1. Applicants respectfully request therefore that the rejection of claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Cohen et al. in view of Le Croy be withdrawn and the claim allowed.

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Although not identical, claim 11 recites features similar to those of claim 1 and, thus, is likewise subject to rejection for at least the reasons set forth above with respect to claim 1.

Claims 5-9 depend upon claim 1 either directly or indirectly and, thus, are likewise not subject to rejections for at least the reasons set forth above with respect to claim 1.

The Office Action at page 3 sets forth "claims 2-4, 10 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cohen et al. and Le Croy as applied to claim 1 above, and further in view of U.S. Patent No. 6,218,848 to Hembree et al." Applicants respectfully submit that this rejection is overcome by the amendments to the claims for the reasons set forth below.

Hembree et al. is relied upon as "[disclosing] a probe apparatus with multiple probes for testing a circuit chip..." Office Action at page 3. Hembree et al., fails to disclose or suggest, however, a single probe apparatus comprising a single probe group having two or more probes with the two or more probes having a common contacting center within a probe target area allowing a test path resistance of the single test terminal of the circuit chip to be measured based solely between the probes of the single probe group. Thus, Hembree et al. fails to make up for the deficiencies of Cohen et al. and Le Croy. Applicants respectfully request therefore that the rejection of claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Cohen et al. and Le Croy and further in view of Hembree et al. be withdrawn and the claim allowed.

Claims 3 and 4 depend upon claim 2 and, thus, are likewise not subject to rejection for at least the reasons set forth above with respect to claim 2. Further, because claims 10 and 12 depend upon claims 1 and 11, respectively, they are likewise not subject to rejection for at least the reasons set forth above with respect to their respective independent claims.

Applicants respectfully therefore that the rejection of claims 3, 4, 10 and 12 be withdrawn and the claims allowed.

Applicants have added claims 13-15. Basis for these claims may be found in Applicants' specification at page 9, lines 24-28 and pages 15, lines 11-28. No new matter has been added. Applicants respectfully request that claims 13-15 be entered and examined.

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In view of the amendments and remarks set forth above, Applicants submit that the above-identified application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

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The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

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<u>June 24, 2004</u>

Kathleen Carney